

1 **In the claims:**

2 1. A method for in-line error detection and correction using wires 0 to  $k-1$ ,  
3 and symbols 0 to  $n$ , said method comprising steps of:

4 calculating a horizontal parity (HP[i]) for  $i=0$  to  $n-2$ , where  $n$  is a number of

5 symbols used, and  $HP[i] = \bigoplus_{x=0}^{k-1} b[x][i]$ , and  $k$  is a number of wires used;

6 calculating an extended parity (EP) =  $\sum_{x=0}^{k-1} \sum_{y=0}^{n-1} b[x][y] \alpha^{(x+y+B)}$ , where  $B$  a degree of

7 primitive polynomial+1 and a number of bits in a syndrome;

8 sending contents of the horizontal parity along wire 0 of  $k$  wires, where HP[0] is  
9 in symbol 0, HP[1] is in symbol 1, ..., HP[n-2] is in symbol  $n-2$ ;

10 calculating an overall parity (OP) where the OP is an exclusive-or of the  
11 horizontal and extended parities;

12 sending check bits along the wires in symbol 0, wherein the check bits comprise  
13 the extended parity, the horizontal parity and the overall parity;

14 sending information bits in symbols 1.. $n-1$ , wherein symbol[i] carries bits  
15  $b[k-1..0][i]$ ;

16 determining whether check bits have an error;

17 calculating a syndrome 0 and a syndrome 1, wherein syndrome 0 is a  $B$ -bit

18 quantity  $\{eB-1, \dots, e2, e1, e0\}$  such that  $e[i] = \bigoplus_{x=0}^k b[x][i+1] \oplus HP[i]$ , where  $HP[i] =$

19  $b[i+1][0..7]$ , and wherein syndrome 1 is a summation of the extended parity and seven  
20 degree polynomial;

21 determining whether bit  $i$  in wire  $j$  contains an error; and

22 if bit  $i$  in wire  $j$  contains an error, then fixing the bit error by flipping the  
23 erroneous bit.

24 2. A method for in-line error detection and correction using wires 0 to  $k-1$ ,  
25 and symbols 0 to  $n$ , where information bits and symbols are sent along wires 0 to  $k$ , said  
26 method comprising steps of:

27 calculating check bits from information bits, wherein the check bits comprise  
28 horizontal parity, extended parity and overall parity of the information;

29 sending the check bits along wires 0 to  $k-1$ , wherein information is sent along the  
30 same wires;

1            determining whether an error exists in the sent information using syndromes  
2    generated from the check bits, wherein syndrome 0 is obtained from the horizontal parity  
3    (HP) bits by taking an exclusive-OR (XOR'ing) of the information bits with the HP bits  
4    and wherein syndrome 1 comprises a degree  $n - 1$  polynomial; and

5            correcting single wire errors determined using the syndromes.

6            3.        The method as recited in claim 2, wherein the horizontal parity (HP[i]), for

7     $i=0$  to  $n-2$ , is  $HP[i] = \bigoplus_{x=0}^{k-1} b[x][i]$ , where  $n$  is a number of symbols used, and  $k$  is a number  
8    of wires used, and wherein the extended parity (EP) is  $\sum_{x=0}^{k-1} \sum_{y=0}^{n-1} b[x][y] \alpha^{(x+y+B)}$ , where  $B$  a  
9    degree of primitive polynomial + 1 and a number of bits in a syndrome.

10          4.        The method as recited in claim 3, wherein contents of the horizontal parity  
11    are sent along wire 0 of  $k$  wires, where  $HP[0]$  is in symbol 0,  $HP[1]$  is in symbol 1, ...,  
12    and  $HP[n-2]$  is in symbol  $n-2$ .

13          5.        An apparatus for in-line error detection and correction using wires 0 to  $k-1$ ,  
14    and symbols 0 to  $n$ , comprising:

15            an encoder for calculating a horizontal parity (HP), extended parity (EP) and  
16    overall parity (OP) for information bits, wherein the horizontal parity (HP[i]) for  $i=0$  to  
17     $n-2$ , where  $n$  is a number of symbols used, and  $HP[i] = \bigoplus_{x=0}^k b[x][i]$ , and  $k$  is a number of  
18    wires used, and wherein the extended parity (EP) =  $\sum_{x=0}^{k-1} \sum_{y=0}^{n-1} b[x][y] \alpha^{(x+y+B)}$ , where  $B$  a  
19    degree of primitive polynomial+1 and a number of bits in a syndrome, and wherein the  
20    overall parity (OP) is an exclusive-or of the HP and the EP;

21            means for sending the information bits and calculated parity bits across wires 0 to  
22     $k$ , wherein check bits are sent along the wires in symbol 0, wherein the check bits  
23    comprise the extended parity, the horizontal parity and the overall parity, and wherein  
24    information bits are sent in symbols 1.. $n-1$ , where symbol[i] carries bits  $b[k-1..0][i]$ , and  
25    wherein horizontal parity (HP) is sent along wire 0, where  $HP[0]$  is in symbol 0,  $HP[1]$  is  
26    in symbol 1, ...,  $HP[n-2]$  is in symbol  $n-2$ ;

27            means for determining whether check bits have an error, comprising decoder for  
28    calculating a syndrome 0 and a syndrome 1, wherein syndrome 0 is a  $B$ -bit quantity { $eB-$   
29     $I, \dots, e2, e1, e0$ } such that  $e[i] = \bigoplus_{x=0}^{17} b[x][i+1] \oplus HP[i]$ , where  $HP[i] = b[i+1][0..7]$ , and

1 wherein syndrome 1 is a summation of the extended parity and seven degree polynomial;  
2 and

3 means for fixing bit errors determined by the determining means.

4 6. An apparatus for in-line error detection and correction using wires 0 to  $k-1$ ,  
5 and symbols 0 to  $n$ , comprising:

6 an encoder for calculating check bits from information bits, wherein the check bits  
7 comprise horizontal parity, extended parity and overall parity of the information;

8 a transmitter for sending the check bits along wires 0 to  $k-1$ , wherein information  
9 is sent along the same wires;

10 means for determining whether an error exists in the sent information using  
11 syndromes generated from the check bits, wherein syndrome 0 is obtained from the  
12 horizontal parity (HP) bits by taking an exclusive-OR (XOR'ing) of the information bits  
13 with the HP bits and wherein syndrome 1 comprises a degree  $n-1$  polynomial; and

14 error correction component for correcting single wire errors determined using the  
15 syndromes.

16 7. The apparatus as recited in claim 6, wherein the horizontal parity (HP[i]),

17 for  $i=0$  to  $n-2$ , is  $HP[i] = \bigoplus_{x=0}^k b[x][i]$ , where  $n$  is a number of symbols used, and  $k$  is a

18 number of wires used, and wherein the extended parity (EP) is  $\sum_{x=0}^{k-1} \sum_{y=0}^{n-1} b[x][y] \alpha^{(x+y+B)}$ ,

19 where  $B$  a degree of primitive polynomial + 1 and a number of bits in a syndrome.

20 8. The apparatus as recited in claim 7, wherein contents of the horizontal  
21 parity are sent along wire 0 of  $k$  wires, where  $HP[0]$  is in symbol 0,  $HP[1]$  is in symbol 1,  
22 ... , and  $HP[n-2]$  is in symbol  $n-2$ .